What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a tower-like gate pillar formed on said semiconductor substrate via an insulation layer, said gate pillar including a channel region formed so as to be positioned between impurity diffusion regions in a layering direction;

a gate insulation film formed on an outer surface of said gate pillar; and

a gate electrode film formed on an outer surface of said gate insulation film;

wherein said gate electrode film is formed of a plurality of layers each formed in order from said gate pillar, in the direction where said gate electrode film is formed.

2. A semiconductor device comprising:

a semiconductor substrate;

a tower-like gate pillar formed on said semiconductor substrate via an insulation layer, wherein said gate pillar includes a channel region formed so as to be positioned between impurity diffusion regions in a layering direction;

a gate electrode film formed so as to enclose the outer circumferential side of said gate pillar; and

a gate insulation film formed between said gate pillar and said gate electrode film;

wherein said gate electrode film includes a first electrode film formed as to enclose said gate pillar from a circumferential direction thereof, and a second electrode film formed so as to enclose said first electrode film from a peripheral side thereof.

3. The semiconductor device according to claim 1, wherein:

a wiring layer is formed on said gate electrode film on a side of said substrate;

said gate electrode film includes a first electrode film and a second electrode film formed on an outer circumferential side of said first electrode film; and

said first electrode film has an end thereof spaced from said wiring layer, and said second electrode film is formed so as to electrically connect with said wiring layer.

4. The semiconductor device according to claim 1, wherein:

said gate electrode film includes a first electrode film and a second electrode film formed on an outer circumferential side of said first electrode film; and

an end of said first electrode film is formed so as to be more spaced from said semiconductor substrate than an end of said second electrode film.

5. The semiconductor device according to claim 2,

wherein said first electrode film is formed more thinly than said second electrode film.

6. The semiconductor device according to claim 2, wherein said first electrode film is formed with a grain size smaller than that of said second electrode film.

7. The semiconductor device according to claim 2, wherein said first electrode film and said second electrode film each include a polycrystalline silicon film.

8. The semiconductor device according to claim 2, wherein said first electrode film is a polycrystalline silicon film and said second electrode film is a conductive film containing a metal element.

9. The semiconductor device according to claim 2, wherein said channel region is formed with a grain size greater than that of said first electrode film or said second electrode film.

10. A method of manufacturing a semiconductor device, comprising:

a step of forming, on a semiconductor substrate via an insulation layer, a tower-like gate pillar in which a channel region is formed so as to be positioned between impurity diffusion regions in a layering direction;

a step of forming a gate insulation film so as to enclose an outer circumferential side of said gate pillar; and

a step of forming a gate electrode film so as to

enclose an outer circumferential side of said gate insulation film;

wherein said step of forming said gate electrode film further includes:

a step of forming an amorphous first silicon layer so as to enclose said gate pillar from a circumferential direction thereof;

a step of thermally treating said silicon layer formed in said step;

a step of forming a polycrystalline second silicon layer so as to enclose said first electrode layer from an outer circumferential side thereof; and

a step of thermally treating said electrode layer.